

## CLAIMS

What is claimed is:

1. A method of preventing charge buildup during fabrication of a semiconductor device, the method comprising:

5 coupling a first transistor to a first metal wire on a first metal level of a semiconductor device, the first transistor being configured to protect a gate of a second transistor from charge buildup, a gate of the first transistor being left floating;

forming a second metal wire in the device; and

switching ON the first transistor to discharge charges accumulated on the first  
10 metal wire during formation of the second metal wire.

2. The method of claim 1 further comprising:

coupling the gate of the first transistor to ground on a topmost metal level of the device.

3. The method of claim 1 wherein the second metal wire is on a second metal level  
15 of the device, the second metal level being over the first metal level.

4. The method of claim 1 wherein coupling the first transistor to the first metal wire comprises:

connecting a drain of the first transistor to the first metal wire;

connecting a source of the first transistor to ground; and

20 connecting the gate of the first transistor to the metal wire by way of a coupling capacitor.

5. The method of claim 4 wherein a value of the coupling capacitor is selected by design to switch ON the first transistor at a predetermined gate voltage.

6. The method of claim 1 wherein the second metal wire is formed by physical vapor deposition.

5 7. The method of claim 1 wherein the second transistor comprises an MOS transistor.

8. The method of claim 1 further comprising:

forming a second metal level over the first metal level;

forming a third metal level over the second metal level; and

10 coupling the gate of the first transistor to a third metal wire on the third metal level by way of a plurality of vertically stacked vias.

9. The method of claim 8 wherein the third metal wire is connected to ground.

10. The method of claim 2 wherein the topmost metal level is a second metal level over the first metal level.

15 11. The method of claim 1 wherein the first transistor comprises an nfet.

12. A circuit for preventing charge buildup on an interconnect line during a metallization process, the circuit comprising:

a first transistor, a drain of the first transistor being coupled to the interconnect

line, a source of the first transistor being coupled to ground, and a gate of the first

20 transistor being left floating; and

a capacitor coupling the gate of the first transistor to the interconnect line, the capacitor having a value selected to switch ON the first transistor and protect a gate of a second transistor when charges accumulate on the interconnect line during a metallization process.

5 13. The circuit of claim 12 wherein the first transistor protects the gate of the second transistor from charge buildup on the interconnect line due to physical vapor deposition.

14. The circuit of claim 12 wherein the first transistor comprises an nfet.

15. The circuit of claim 12 wherein the first transistor comprises an nfet and the second transistor comprises a MOS transistor.

10 16. The circuit of claim 12 wherein the interconnect line is on a first metal level and the gate of the first transistor is coupled to ground on a topmost metal level over the first metal level.

17. The circuit of claim 16 further comprising a plurality of vertically stacked vias coupling the interconnect line to the ground on the topmost metal level.

15 18. A method of protecting an integrated circuit gate during a metallization process, the method comprising:

switching ON a first transistor to discharge charges accumulated on an interconnect line during a metallization process to protect a gate of a second transistor coupled to the interconnect line, a gate of the first transistor being left floating during the  
20 metallization process.

19. The method of claim 18 further comprising:

coupling the gate of the first transistor to ground after the metallization process.

20. The method of claim 18 wherein the metallization process comprises physical vapor deposition.